β

EXAMPLE 3.1

(a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
(b) Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
(c) Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
(d) Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution

(a) The characteristics clearly indicate that $I_C \cong I_E = \mathbf{3\ mA}$.
(b) The effect of changing V_{CB} is negligible and I_C continues to be **3 mA.**
(c) From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V.**
(d) Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c, V_{BE} is **0.7 V** for any level of emitter current.

Alpha (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \tag{3.5}$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that $\alpha = 1$, for practical devices the level of alpha typically extends from 0.90 to 0.998, with most approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes

$$I_C = \alpha I_E + I_{CBO} \tag{3.6}$$

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, I_C also appears to be 0 mA for the range of V_{CB} values.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}\ =\ \text{constant}} \tag{3.7}$$

The ac alpha is formally called the *common-base, short-circuit, amplification factor,* for reasons that will be more obvious when we examine transistor equivalent circuits in Chapter 7. For the moment, recognize that Eq. (3.7) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other. The use of an equation such as (3.7) will be demonstrated in Section 3.6.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $I_C \cong I_E$ and assuming for the moment that

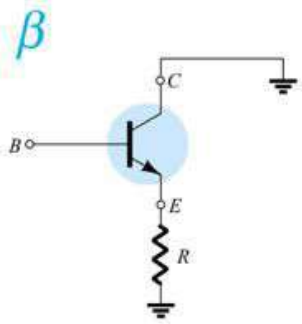

Figure 3.21 Common-collector configuration used for impedance-matching purposes.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.6. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{EC} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

3.8 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics which will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as *continuous* collector current) and maximum collector-to-emitter voltage (often abbreviated as V_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{C_{max}}$ was specified as 50 mA and V_{CEO} as 20 V. The vertical line on the characteristics defined as $V_{CE_{sat}}$ specifies

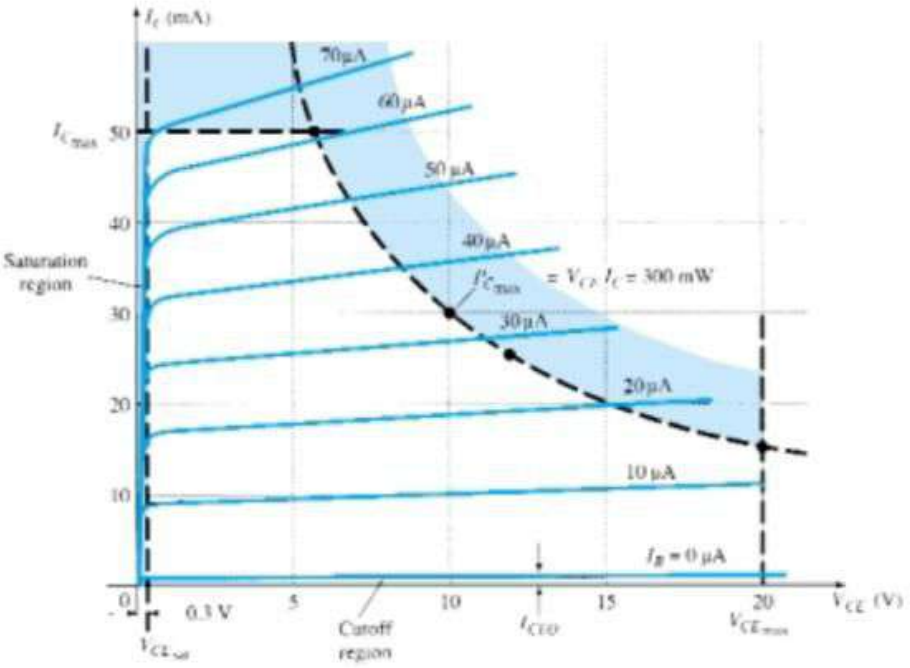

Figure 3.22 Defining the linear (undistorted) region of operation for a transistor.

the minimum V_{CE} that can be applied without falling into the nonlinear region labeled the *saturation* region. The level of $V_{CE_{sat}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.

The maximum dissipation level is defined by the following equation:

$$P_{C_{max}} = V_{CE}I_C \tag{3.16}$$

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{max}} = V_{CE}I_C = 300 \text{ mW}$$

or

$$V_{CE}I_C = 300 \text{ mW}$$

At any point on the characteristics the product of V_{CE} and I_C must be equal to 300 mW. If we choose I_C to be the maximum value of 50 mA and substitute into the relationship above, we obtain

$$V_{CE}I_C = 300 \text{ mW}$$

$$V_{CE}(50 \text{ mA}) = 300 \text{ mW}$$

$$V_{CE} = \frac{300 \text{ mW}}{50 \text{ mA}} = \mathbf{6\ V}$$

As a result we find that if $I_C = 50$ mA, then $V_{CE} = 6$ V on the power dissipation curve as indicated in Fig. 3.22. If we now choose V_{CE} to be its maximum value of 20 V, the level of I_C is the following:

$$(20 \text{ V})I_C = 300 \text{ mW}$$

$$I_C = \frac{300 \text{ mW}}{20 \text{ V}} = \mathbf{15\ mA}$$

defining a second point on the power curve.

If we now choose a level of I_C in the midrange such as 25 mA, and solve for the resulting level of V_{CE}, we obtain

$$V_{CE}(25 \text{ mA}) = 300 \text{ mW}$$

and

$$V_{CE} = \frac{300 \text{ mW}}{25 \text{ mA}} = \mathbf{12\ V}$$

as also indicated on Fig. 3.22.

A rough estimate of the actual curve can usually be drawn using the three points defined above. Of course, the more points you have, the more accurate the curve, but a rough estimate is normally all that is required.

The *cutoff* region is defined as that region below $I_C = I_{CEO}$. This region must also be avoided if the output signal is to have minimum distortion. On some specification sheets only I_{CBO} is provided. One must then use the equation $I_{CEO} = \beta I_{CBO}$ to establish some idea of the cutoff level if the characteristic curves are unavailable. Operation in the resulting region of Fig. 3.22 will ensure minimum distortion of the output signal and current and voltage levels that will not damage the device.

If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE}I_C$ fall into the range appearing in Eq. (3.17).

β

$$I_{CEO} \leqq \boldsymbol{I_C} \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq \boldsymbol{V_{CE}} \leqq V_{CE_{max}} \qquad (3.17)$$
$$\boldsymbol{V_{CE}I_C} \leqq P_{C_{max}}$$

For the common-base characteristics the maximum power curve is defined by the following product of output quantities:

$$P_{C_{max}} = V_{CB}I_C \qquad (3.18)$$

3.9 TRANSISTOR SPECIFICATION SHEET

Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood. Although all the parameters have not been introduced, a broad number will now be familiar. The remaining parameters will be introduced in the chapters that follow. Reference will then be made to this specification sheet to review the manner in which the parameter is presented.

The information provided as Fig. 3.23 is taken directly from the *Small-Signal Transistors, FETs, and Diodes* publication prepared by Motorola Inc. The 2N4123 is a general-purpose *npn* transistor with the casing and terminal identification appearing in the top-right corner of Fig. 3.23a. Most specification sheets are broken down into *maximum ratings, thermal characteristics, and electrical characteristics.* The electrical characteristics are further broken down into "on," "off," and small-signal characteristics. The "on" and "off" characteristics refer to dc limits, while the small-signal characteristics include the parameters of importance to ac operation.

Note in the maximum rating list that $V_{CE_{max}} = V_{CEO} = 30$ V with $I_{C_{max}} = 200$ mA. The maximum collector dissipation $P_{C_{max}} = P_D = 625$ mW. The derating factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1° rise in temperature above 25°C. In the "off" characteristics I_{CBO} is specified as 50 nA and in the "on" characteristics $V_{CE_{sat}} = 0.3$ V. The level of h_{FE} has a range of 50 to 150 at $I_C = 2$ mA and $V_{CE} = 1$ V and a minimum value of 25 at a higher current of 50 mA at the same voltage.

The limits of operation have now been defined for the device and are repeated below in the format of Eq. (3.17) using $h_{FE} = 150$ (the upper limit) and $I_{CEO} \cong \beta I_{CBO} = (150)(50\text{ nA}) = 7.5\ \mu\text{A}$. Certainly, for many applications the 7.5 μA = 0.0075 mA can be considered to be 0 mA on an approximate basis.

Limits of Operation

$$7.5\ \text{mA} \leqq \boldsymbol{I_C} \leqq 200\ \text{mA}$$
$$0.3\ \text{V} \leqq \boldsymbol{V_{CE}} \leqq 30\ \text{V}$$
$$\boldsymbol{V_{CE}I_C} \leqq 650\ \text{mW}$$

In the small-signal characteristics the level of h_{fe} (β_{ac}) is provided along with a plot of how it varies with collector current in Fig. 3.23f. In Fig. 3.23j the effect of temperature and collector current on the level of h_{FE} (β_{ac}) is demonstrated. At room temperature (25°C), note that h_{FE} (β_{dc}) is a maximum value of 1 in the neighborhood of about 8 mA. As I_C increased beyond this level, h_{FE} drops off to one-half the value with I_C equal to 50 mA. It also drops to this level if I_C decreases to the low level of 0.15 mA. Since this is a *normalized* curve, if we have a transistor with $\beta_{dc} = h_{FE} = 50$ at room temperature, the maximum value at 8 mA is 50. At $I_C = 50$ mA it has dropped to 50/2 = 25. In other words, normalizing reveals that the actual level of h_{FE}